
RS485 Facts and Bus

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October 2019

The following document collects the most important facts about the RS485 standard together with background information (▲) to understand what is behind these features. This information leads to guidelines (▶) for a correct connection of the complete system. Some hints to connection traps (▼) complement the chapters. Read the chapters in their sequence as they are relating to each other. A summary for the connection guidelines and some bus schematics conclude this article.

Signal type

The RS485 lines are complementary differential signals (A+, B-). A positive voltage difference between A+ and B- is assigned to logical '1' (Idle), a negative voltage to '0'. The bus is called 2-wire bus.

▲ In this way disturbances from the environment, which enter both lines at the same time, shift the line levels simultaneously and do not change the difference voltage.

The receivers are designed for voltage shifts in the range of -7V to +12V, the common mode range, which is $\pm 9.5V$ to the middle of the RS485 bus voltage range of 0 to +5V.

The logical value can still be correctly decoded when the bus gets a shifting impact.

▶ To achieve this optimally the data wires of equal length have to be twisted so that irradiations enter both wires equally. A shielded bus cable further helps to keep out disturbances, especially in rough environment.

▼ Make sure that you place the bus in an as clean as possible environment. For example placing it side by side with a motor supply cable will cause undefined errors because of the high and changing electromagnetic field.

Ground line

Because only the voltage differences are measured the ground line could be omitted.

▲ This only works for ideal environment. If equalizing currents arise they have to flow

through the data lines instead of the balancing ground line. These currents can come from long buses, different power supplies for the devices, disturbances from outside and many other reasons. Undefined errors are the result, especially for higher bit rates.

In addition the receivers internally need a ground to decode the signal, even if it is a voltage difference. If no ground line is present they generate an unstable and fluctuating virtual ground which is different to a real ground.

▶ The recommendation is: Don't 'optimize' the ground wire away, connect all bus participants with ground, make the 2-wire bus a 3-wire one. If you need a floating bus device use a RS485 isolator.

▼ Some devices do not offer a ground connection for whatever reason. Consider to replace them for other types or connect to their internal ground.

Bus topology

The bus wires must be routed from device to device without significant stubs. It is not recommended to use a straight backbone with more or less long branch lines.

▲ At the end of every stub wire the signal is reflected and runs back to the main bus. These reflections are delayed depending on the length of the stub and will interfere with the original signal. The results are distorted signals and therewith unclear bits.

▶ Wire the bus from device to device. There must be only two ends, no branch lines.

▼ If you split the bus into segments by adding repeaters or isolators make sure that every segment has its own correct topology.

Especially the termination and biasing resistors (see next chapters) have to be doubled.

Bus termination

Both bus ends have to be terminated through one resistor each between A+ and B-.

▲ As mentioned in the 'bus topology' part the signal is reflected at the end of the bus wires

and runs back and forth again on the line, causing distorted signals. To avoid this the signal reflections must be damped at both wire ends. This is done by 'burning' the energy in resistors between the data lines.

The standard value is 120Ω for each resistor, resulting in 60Ω total resistance between both data lines. The power rating is $0.25W$.

Some devices offer a switch to enable a termination resistor for use in case they are the first or last device on the bus.

► Terminate both bus ends with $120\Omega/0.25W$ resistors between the data lines.

▼ Make sure that exactly two resistors are wired and no device between the ends has its bus termination unintentionally activated, e.g. a former bus end device. That would result in high bus load and collapsing bus voltages by overcharged bus drivers.

Measure the resistance when the bus is off.

Voltage swing

The differential voltage (swing) is $+200mV$ up to $+5V$ and $-200mV$ down to $-5V$ per definition. The value between $-200mV$ and $+200mV$ is undefined.

▲ When the voltages are too small the receiver chips will not return a reliable logical value, especially in a rough environment. These small voltages occur when the bus is undriven and inactive when no device is sending, all are listening on the bus.

So this inactive bus condition needs a special treatment, the bus biasing, see the next part.

In addition small active bus voltages are very failure-prone and give the hint, that the bus is not correctly designed with too much load.

► Examine the bus voltages with a scope and make sure, that the active bus difference voltages are high enough. Voltages above $+2V$ and below $-2V$ are recommended.

▼ Small voltage swings (sometimes only from one weak device) are a hint that the bus is overloaded. Consider splitting the bus into segments with repeaters.

Bus biasing

A bus pull up and down resistor is necessary to set the voltage when the bus is floating (no sender is active).

▲ The bus voltages in the inactive state has to be set for some reasons. The main reason is that the receivers do not detect voltages between $\pm 200mV$ reliably as fail save '1'. Both data lines are nearly shorted through the two 120Ω resistors with a voltage difference of $0V$.

The detected logic level must be equal to the idle state which is logical '1'. If instead a logical '0' would be read it would lead to a break condition and no start bit can be recognized, because the first falling edge would not be seen.

So the bus voltage must be set to a value a bit greater than $+200mV$. This is done by adding a pull up of 680Ω from A+ to $+5V$ and a pull down of 680Ω from B- to ground. Together with the $2 \times 120\Omega$ termination resistors the resulting voltage is a bit over $+200mV$.

Another reason for the biasing (with equal resistors) is that the bus is fixed in the middle of the $5V$ working range at $2.5V$. In this way the level shift range is optimally placed in the common mode range, see chapter 'signal type'. In the floating state the bus sensitivity for disturbances is much higher than in the actively driven state.

► Add a 680Ω resistor anywhere from A+ to $+5V$ and 680Ω from B- to ground. For a long distance bus use 1300Ω resistors instead, but on both ends of the bus, for a more smooth current distribution.

▼ The biasing is often neglected and omitted. This works until the first inexplicable error occurs.

Some devices have internal pull up and down resistors in the $k\Omega$ range. And the input resistors of the devices also change the levels. So measure the rest voltage when the bus is quiet and adapt the resistor values if necessary.

Bus length

The maximum bus length must fit to the maximum bit rate. If the rate is too high the bus must be divided into segments.

▲ The twisted bus cable has a quite high impedance and capacitance which lead to distorted signal edges and bits. The longer the bus the lower the maximum bit rate can be.

Bit rates of up to $100kbps$ can be transferred up to $1km$ in an ideal environment. For higher bit rates the length decreases fast, consult respective tables. To have more immunity simply half the mentioned bus length for a given bit rate.

► Measure the real bus length and consider using repeaters to reinforce the signal and improve the quality if the bus is too long for the given maximum bit rate.

▼ Especially rough environment can decrease the acceptable range significantly. Use the highest bit rate when bus devices can switch the rate under operating conditions.

Bus load

For the attached sending devices the bus is a high load with its termination and biasing resistors. All bus participants additionally increase the load with their input resistors.

▲ A short calculation for the minimum resistance between A+ and D- is around 52Ω . This includes the termination resistors, the pull up/down resistors and the maximum allowed bus devices (32 devices at the standard $12k\Omega$ (unit load) input resistance each). For the minimum recommended voltage swing of $\pm 2V$ the current is $\pm 38mA$.

This current has to be delivered by the drivers at the maximum bit rate and bus impedance.

► Not all devices have sufficient drivers under all circumstances. The best is to capture the bus with a digital scope and check the outputs of all devices. Make sure that all voltages are inside the recommended range. Measure the parallel resistance in the inactive bus state.

▼ The switching behavior can depend on many parameters which must be checked and probably have not be taken into account. The total parallel resistance of the devices, the bus

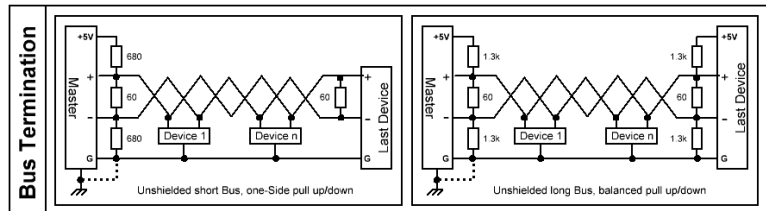
length and bit rate, the power supply of the bus drivers, the environment and a lot more.

Summary

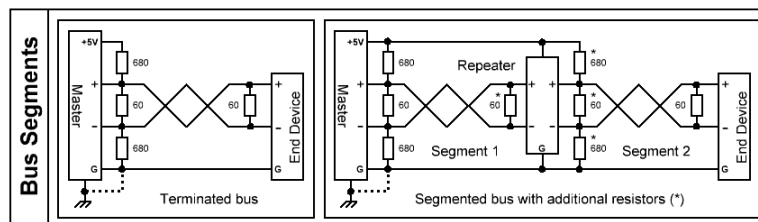
This part sums up the above chapters for correct bus design:

- Use twisted wire pairs of equal length.
- For rough environment use shielded cables
- Use a ground line for all devices.
- Wire from device to device, no stubs.
- Terminate at both bus ends with 120Ω between A+ and B-.
- Make sure (measure) that the termination resistance of the unpowered bus is 60Ω and not much less.
- Bias the bus to a difference voltage of a bit over $+200mV$ at $2.5V$ against ground.
- Check if the bus speed fits to the bus length even under bad conditions.
- Make sure that the voltage swing is in the range of above $+2V$ and below $-2V$ under all operating conditions.
- Use repeaters if necessary to split the bus into segments to decrease the bus load. Treat every segment as an independent bus

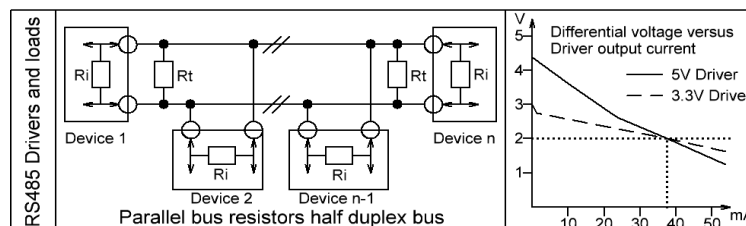
Schematics and diagrams



Basic bus cabling, termination and biasing



Termination and biasing when splitting the bus



Effective load resistors and driver current